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Architecture Highlights

- 15 stage pipeline for 500+ MHz operation.
- Fetch, decode, retire three x86 instructions per cycle.
- Issue up to 9 operations per cycle.
- 7 integer and 3 floating point resources.
- Supports 72 in-flight instructions.
- Deep multi-ported register files.
- High bandwidth, low latency cache subsystem.
- 200 MHz bus.

Technology Summary

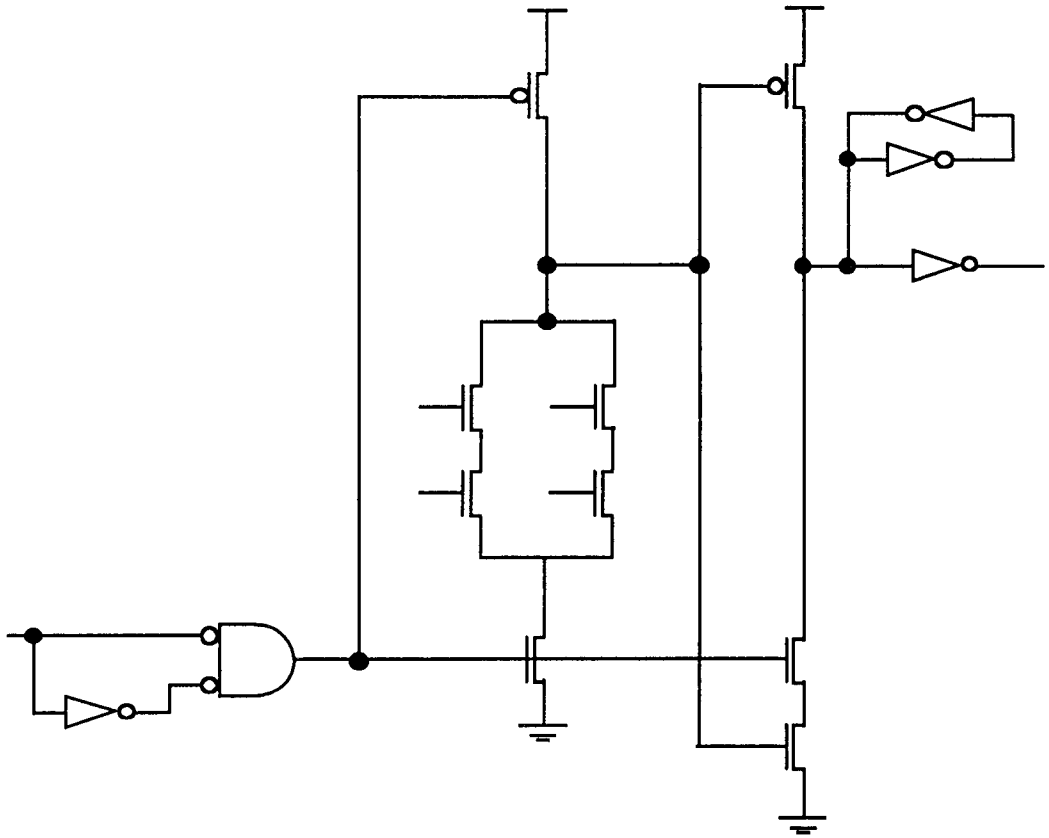
- Power Supply: 1.60 V
- $L_{effective}$: 0.18 µm
- Gate Oxide Thickness: 44 Å
- Local Interconnect Pitch: 0.625 µm
- Metal 1, 2 Pitch: 0.875 µm
- Metal 3 Pitch : 1.000 µm
- Metal 4, 5 Pitch : 1.250 µm
- Metal 6 Pitch : 3.000 µm

Methodology

- Semi-custom design.
- Robust macro cell design.
- Macro cell I/O characterized by in-house tool.
- In-house rule based tool for circuit checks.
- Industry standard tool to check EM and IR.
- Behavorial model used in gate-level simulations.
- Vectors applied to transistor level with dynamic simulator.

Flip-Flops

- Goals:
  - Low latency $T_{DQ.}$
  - Incorporate logic in dynamic stage.

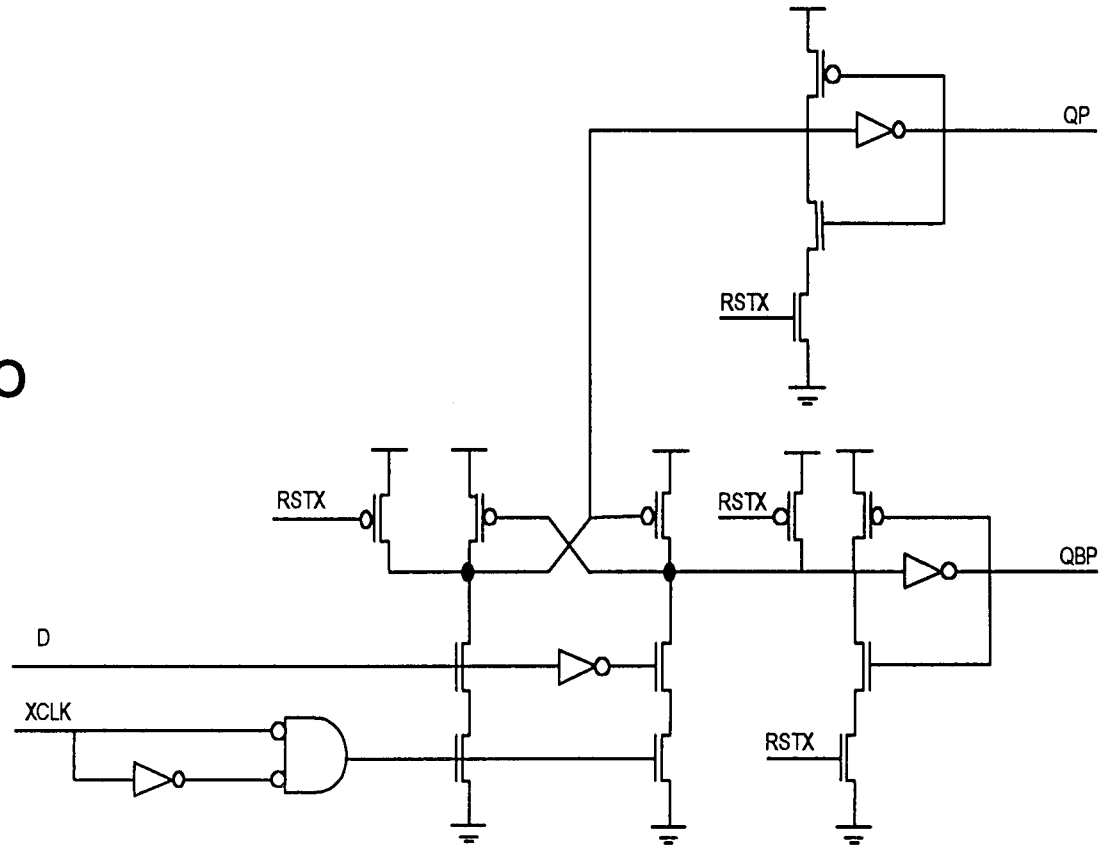


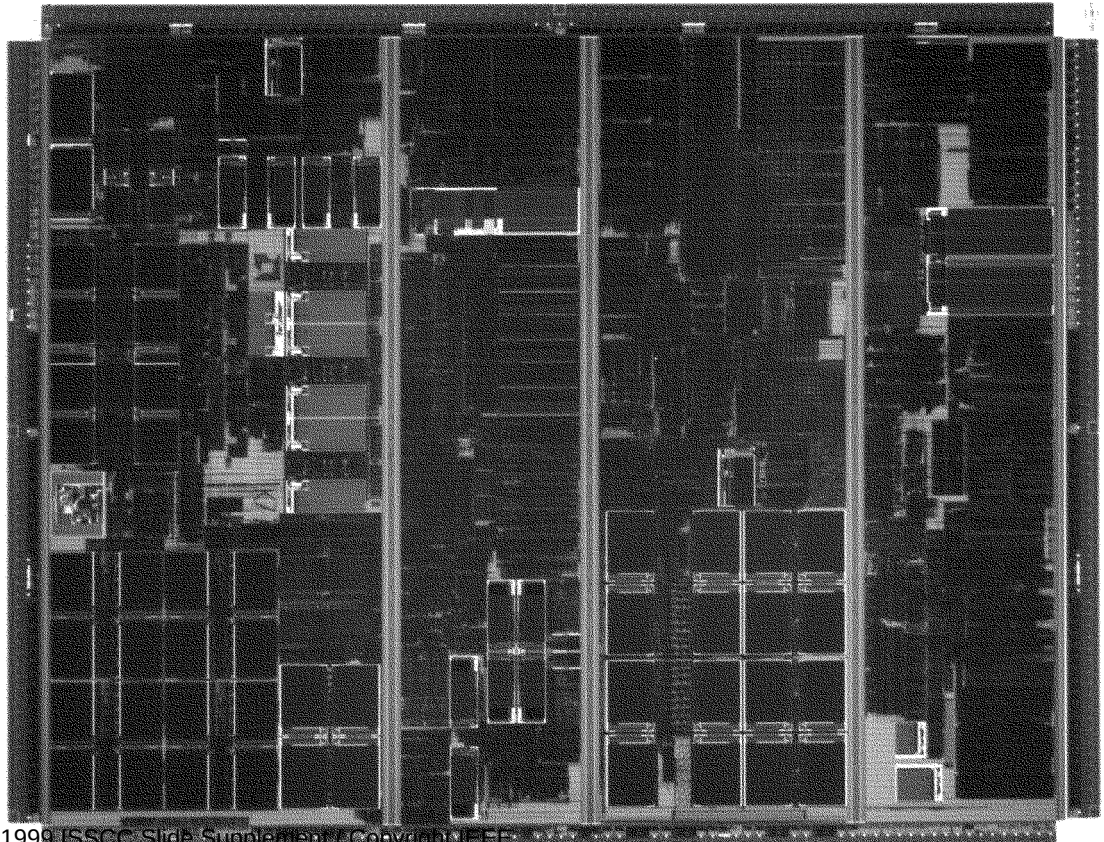
Flip-Flops

- Design Considerations:
  - Dynamic issues.
  - Sensitive to glitches on inputs.
  - Hold time.
  - Clock Load.
- Master-slave flip-flops are used extensively to eliminate hold time concerns and reduce power.

Flip-Flops

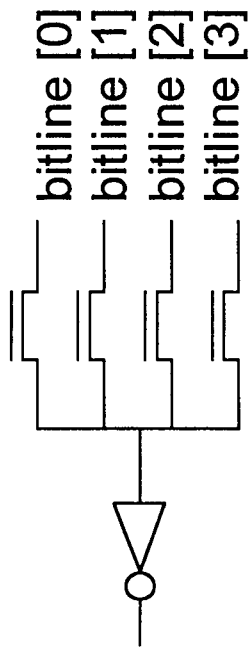
- Dual-rail, monotonic outputs for domino logic.
  - Used only in macro cells.





ROMs

- Bit lines swing full rail.
- Each ROM array is segmented in 64b banks connected by a super bit line.
- Excellent noise immunity.
- Eliminate the risk and complexity of matching circuits and races associated with small signals.



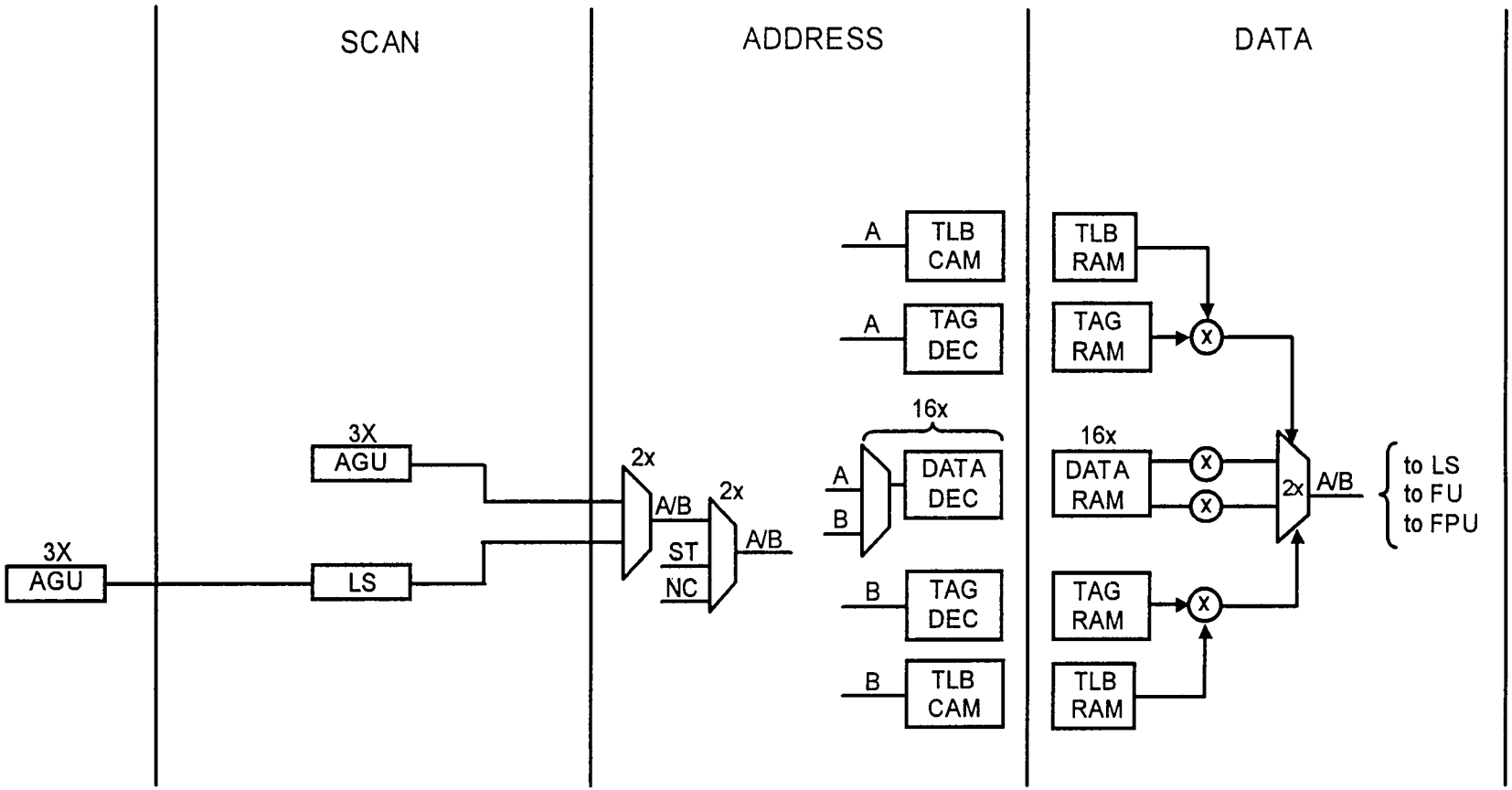
Caches

- Reference bit line for self-timed sense.
- Write pulse can be stretched by clock.
- Static decode, pipelined access in data cache.
- Dynamic decode, single cycle access in instruction cache.
- Access time of all cache macros is less than one cycle.

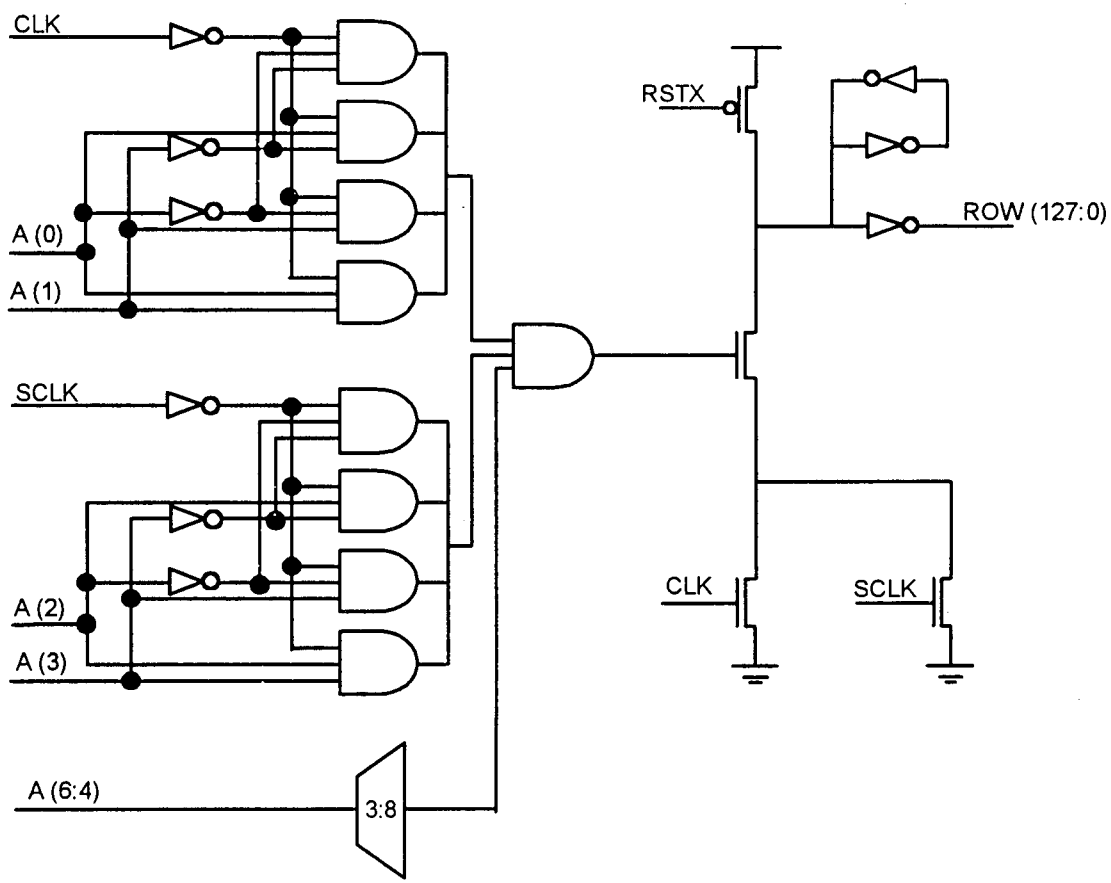
Data Cache

- 64 KB 2-way physically tagged, linearly indexed.
- Bandwidth of 8 GB/sec at 500 MHz.
- 3-cycle load latency.
- Byte writeable.
- Read and write in one cycle.
- 32 entry L1 tlb and 256 entry L2 tlb.

Data Cache Pipeline Diagram



Data Cache Row Decoder

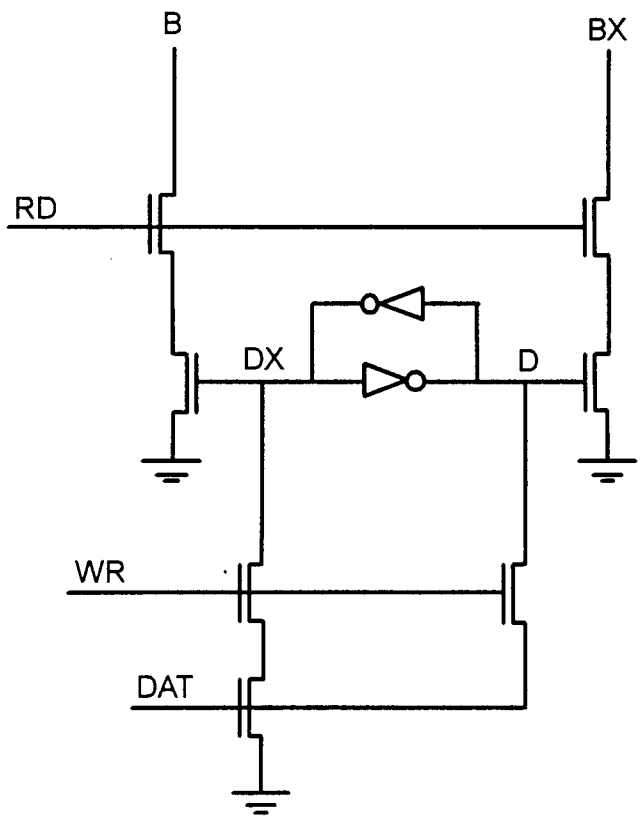


Instruction Cache

- 64 KB 2-way physically tagged, linearly indexed.
- 16 bytes in a fetch window, 64 bytes in a line.
- 64 K entry pre-decode array.
- 2048 entry 2-way branch selector array.
- 1024 entry direct mapped branch target array.
- 32 entry L1 tlb and 256 entry L2 tlb.

Register Files

- Avoid complex bypass circuitry by completing write before read.
- Fast, low voltage writes.

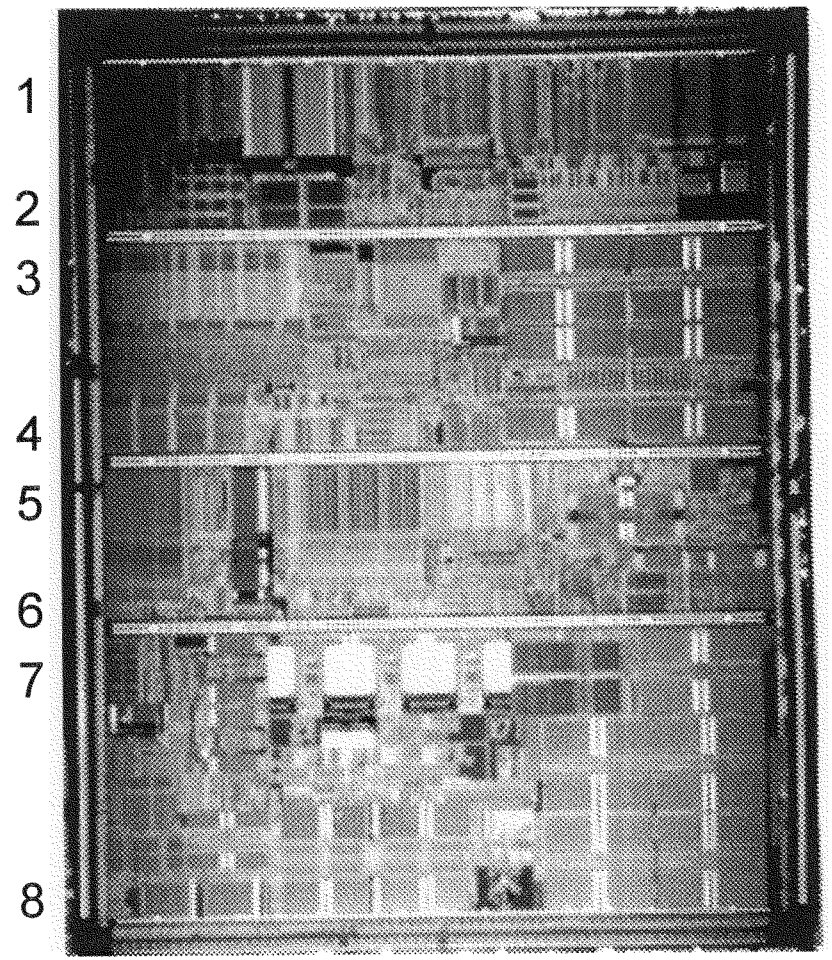


Phase Locked Loop

- Cycle compression <25 ps.
- High precision bandgap to minimize PLL voltage variation.
- Static phase error minimized.
- Extensive test features.

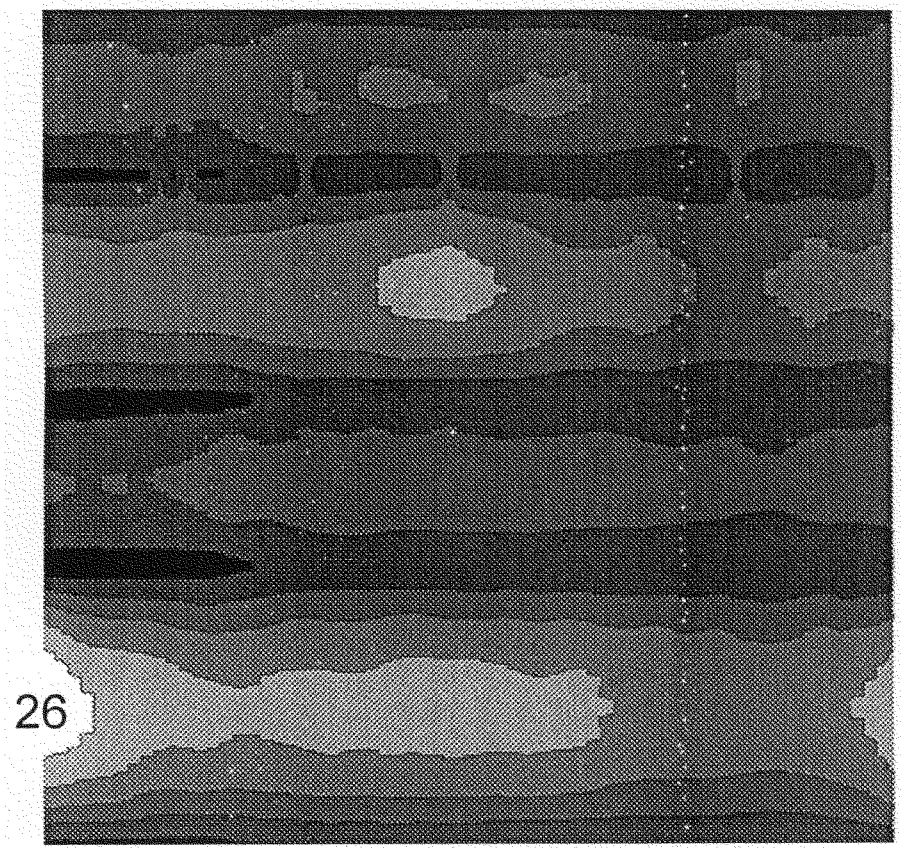
Clock Distribution

- Target Skew: <100 ps (closer to 50 ps).
- RC Skew (est): <30 ps.
- Process Skew (est): <40 ps
- Duty Cycle (est): ±25 ps

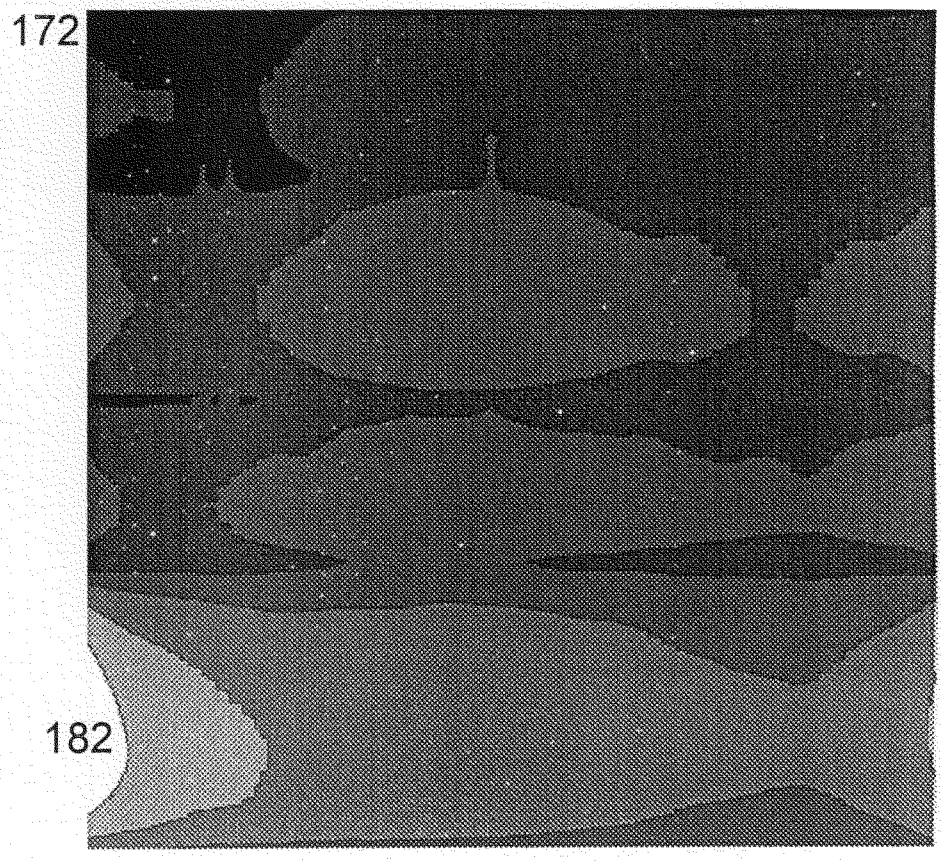


Clock Distribution

- RC Skew (Vdd/2)



- Fall Times (80% to 20%)



I/O

- Software configurable as open drain, push pull, or input-only circuits.
- Source synchronous clocking to minimize skew and delay.
- Deep FIFO to synchronize external data reads with on-chip clock.

Conclusion

- Designed for high-speed operation.
- Semi-custom design.
- Deep multi-ported register files.
- High bandwidth, low latency caches.
- Fast flip-flops.
- Minimize cycle compression and clock skew.
- Robust transistor level design.